Code No: **R32043** **R10** **Set No. 1**

III B.Tech I Semester Supplementary Examinations, Dec - 2015

DIGITAL SIGNAL PROCESSING

(ECE and E Comp E)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1 a) Define causality and stability of an LSI system and state the conditions for stability. [5]

b) Check the linearity, stability, time-invariant and causality for the system described by: [10]

$$y[n] = 2x(n+1) + [x(n-1)]^2$$

2 a) State and prove convolution property of DFT both in time and frequency domain. [8]

b) Find the IDFT of X(k) = {3, (2+j), 1, (2 – j)} [7]

3 a) By showing all the intermediate results, computer the 8-point DFT of the sequence using DIF FFT algorithm: $y(n) = \left\{\frac{1}{2}, \frac{1}{2}, \frac{1}{2}, \frac{1}{2}, 0, 0, 0, 0\right\}$ [8]

b) Draw the flow graph for the decimation-in-frequency FFT algorithm for N=16. What is the number of nontrivial multiplications? [7]

4 a) Determine the frequency response, for the system given by: [8]

$$y[n] - \frac{3}{4}y[n-1] + \frac{1}{8}y[n-2] = x[n] - x[n-1].$$

b) Obtain the cascade and parallel form structures for the following systems described the difference equation: [7]

$$y(n) + 0.1\,y(n-1) - 0.72\,y(n-2) = 0.7\,x(n) - 0.252\,x(n-2)$$

5 a) What is frequency warping? How it can be eliminated in the design of IIR filters using Bi-linear transformation. [8]

b) For the analog transfer function: $H_a(s) = \frac{2}{(s+1)(s+3)}$. Determine H(z) if T=0.5sec using Impulse invariant method. [7]

6 Design an FIR digital filter to approximate an ideal low pass filter with pass band gain of unity, cutoff frequency of 1kHz and working at a sampling frequency f_S=4kHz. The length of the impulse response should be 11. Use Fourier series method. [15]

7 Design single stage and two stage decimator to meet the following specifications: D=100, passband: $0 \le F \le 40$; transition band: $40 \le F \le 50$; input sampling rate: 20,000Hz and ripple: δ_P=0.01, δ_S=0.002. [15]

8 a) Explain special addressing modes in Programmable DSPs. [7]

b) Draw the block diagram of TMS320C50 DSP processor and explain the functionality of CALU and PLU. [8]

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